

General Description

The MY20N02C uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

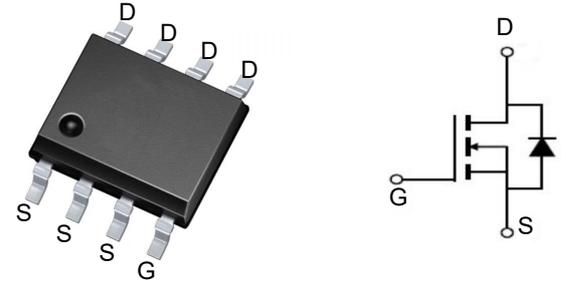


: YUhi fYg

X_{FUU}	20	X
K	20	C
$T_{FUQP} \cdot cXI U? 4.5X+$	4.9	o á
$T_{FUQP} \cdot cXI U? 2.5X+$	7	o á

Application

- Battery protection
- Š[ěÁ, ě&@
- Wj ě ě[] ě ě[, ě ě[] ě



DUW U[Y A Uf]b[UbX CfXYf]b[ěZfa U]cb

DfcXi Wi=8	DUW	A Uf]b[E ěfD7 GŁ
MY20N02C	ÚÚÚĚ	MY20N02C	ĚĚĚĚ

5 Vgc`i ě`AU ja i a `FUě]b[g`fH,1&) °C unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 12	V
$I_{D@Tc=25^{\circ}C}$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	20	A
$I_{D@Tc=100^{\circ}C}$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	15	A
$I_{D@TA=25^{\circ}C}$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	7.3	A
$I_{D@TA=70^{\circ}C}$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	5.8	A
I_{DM}	Pulsed Drain Current ²	50	A
EAS	Single Pulse Avalanche Energy ³	8.1	mJ
I_{AS}	Avalanche Current	12.7	A
$P_{D@Tc=25^{\circ}C}$	Total Power Dissipation ⁴	20.8	W
$P_{D@TA=25^{\circ}C}$	Total Power Dissipation ⁴	2	W
T_{STG}	Storage Temperature Range -	55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	62	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	6	°C/W

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	20	---	---	V
BV _{DSS} /T _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.023	---	V/°C
R _{DS(on)}	Static Drain-Source On-Resistance ²	V _{GS} =4.5V, I _D =10A	---	4.9	6.5	mΩ
		V _{GS} =2.5V, I _D =8A	---	7	9	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	0.4	0.7	1.0	V
V _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-4.2	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±12V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =10A	---	5.5	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	2.3	---	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =15V, V _{GS} =4.5V, I _D =10A	---	4.9	---	nC
Q _{gs}	Gate-Source Charge		---	1.66	---	
Q _{gd}	Gate-Drain Charge		---	1.85	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =15V, V _{GS} =4.5V, R _G =3.3, I _D =10A	---	1.6	---	ns
T _r	Rise Time		---	15.8	---	
T _{d(off)}	Turn-Off Delay Time		---	13	---	
T _f	Fall Time		---	4.8	---	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	416	---	pF
C _{oss}	Output Capacitance		---	62	---	
C _{riss}	Reverse Transfer Capacitance		---	51	---	
I _S	Continuous Source Current ^{1,5}	V _{GS} =V _D =0V, Force Current	---	---	24	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	50	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V
t _{rr}	Reverse Recovery Time	I _F =10A, di/dt=100A/μs, T _J =25°C	---	8.7	---	nS
Q _{rr}	Reverse Recovery Charge	T _J =25°C	---	1.95	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width .The EAS data shows Max. rating .
- 3.he test condition is V_{GS} ≤ 300us , duty cycle $\frac{t_{ON}}{T} \leq 2\%$, V_{GS}=10V, L=0.1mH, I_{AS}=12.7A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

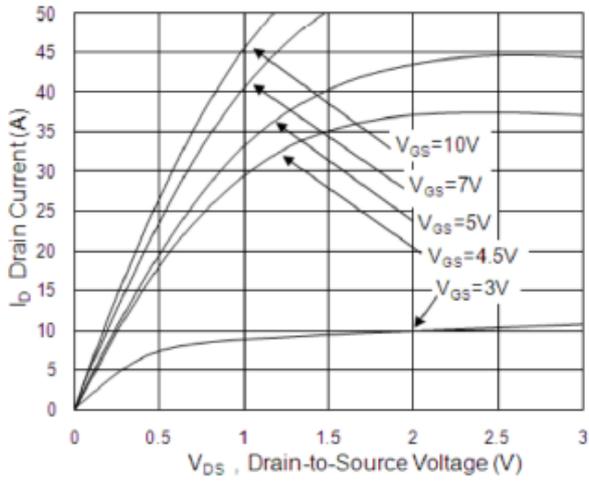


Fig.1 Typical Output Characteristics

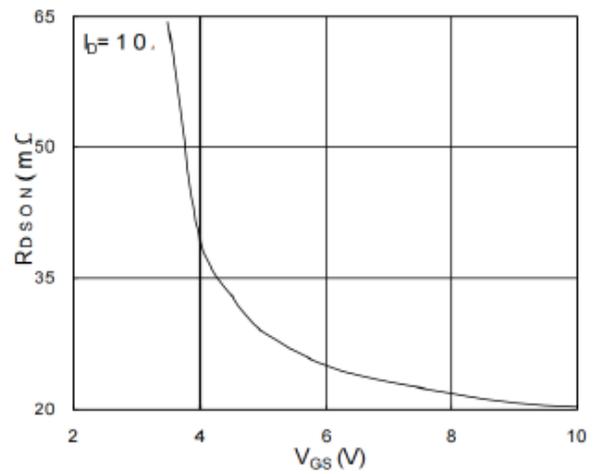


Fig.2 On-Resistance vs. Gate-Source

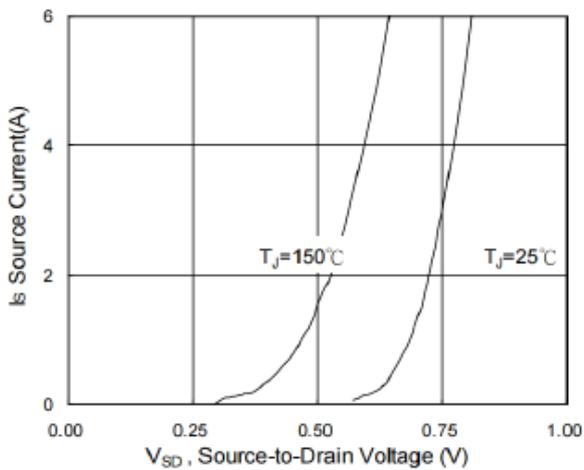


Fig.3 Forward Characteristics Of Reverse

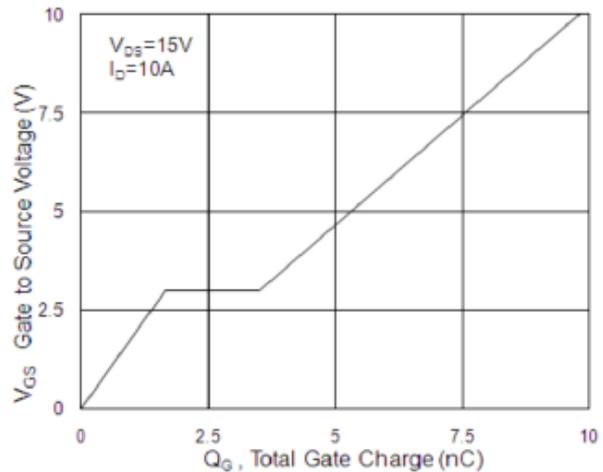


Fig.4 Gate-Charge Characteristics

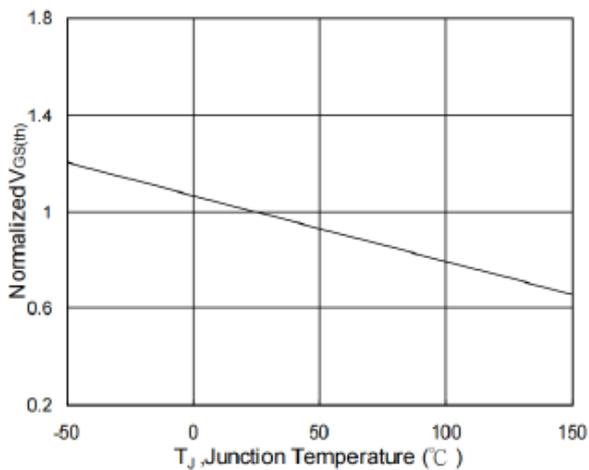


Fig.5 Normalized V_{GS(th)} vs. T_J

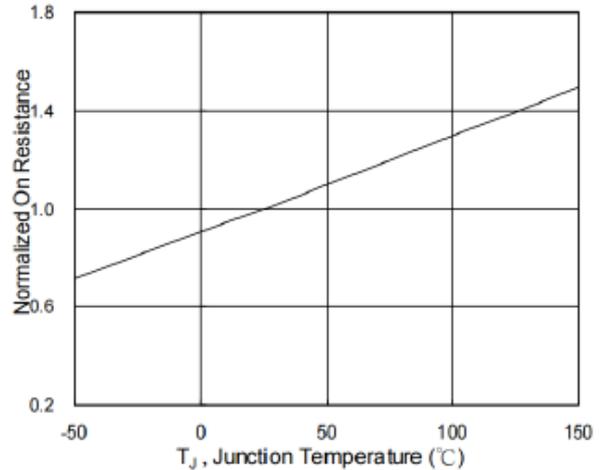


Fig.6 Normalized R_{DS(on)} vs. T_J

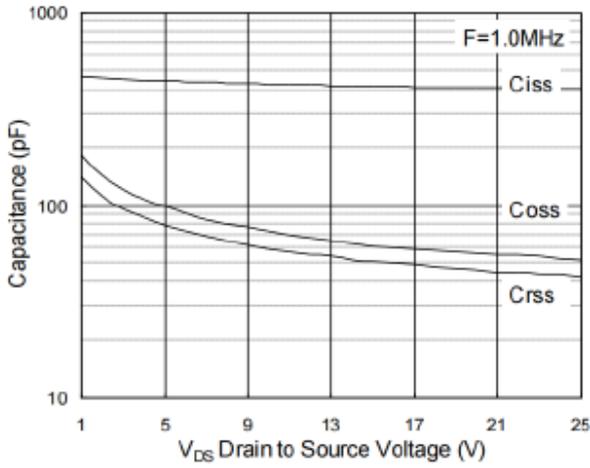


Fig.7 Capacitance

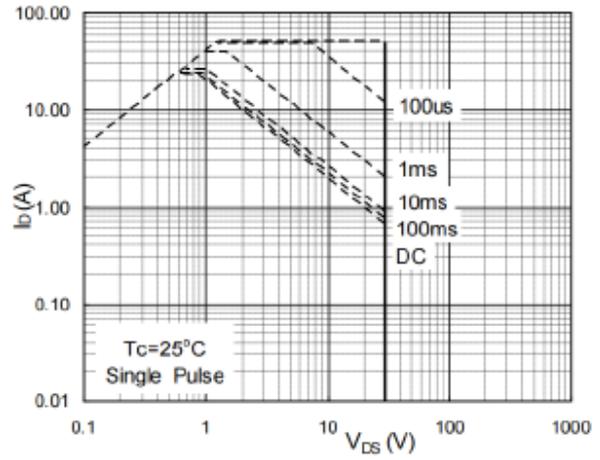


Fig.8 Safe Operating Area

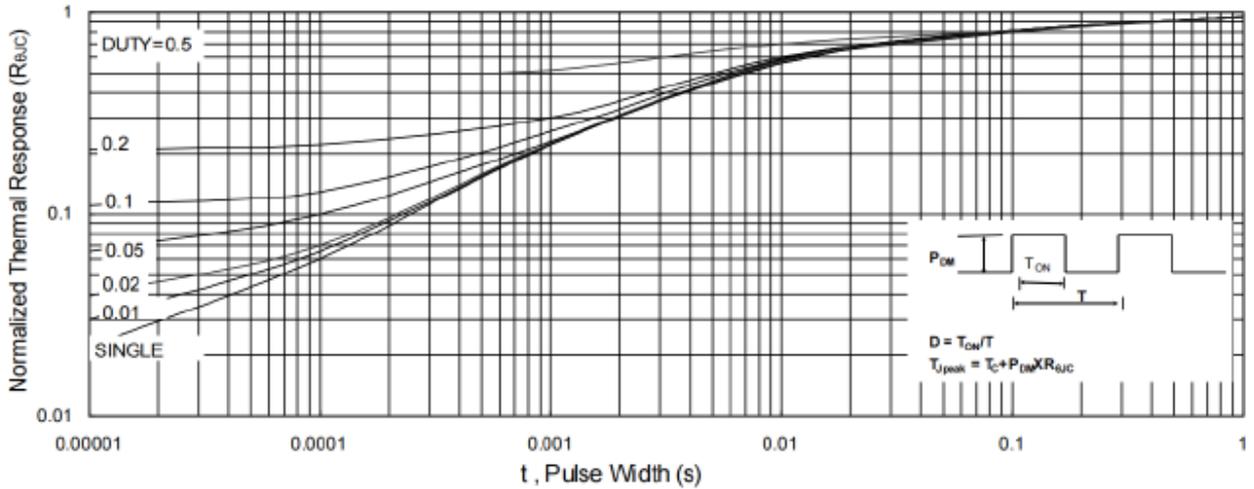


Fig.9 Normalized Maximum Transient Thermal Impedance

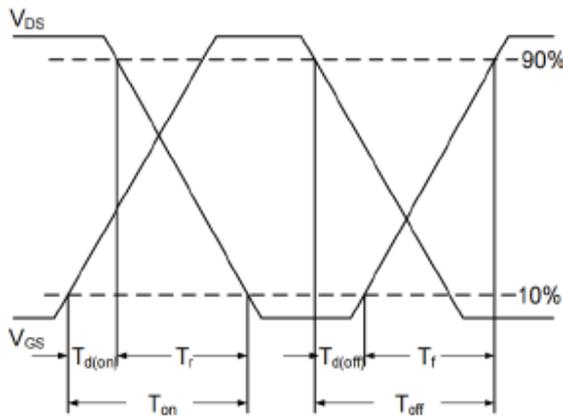


Fig.10 Switching Time Waveform

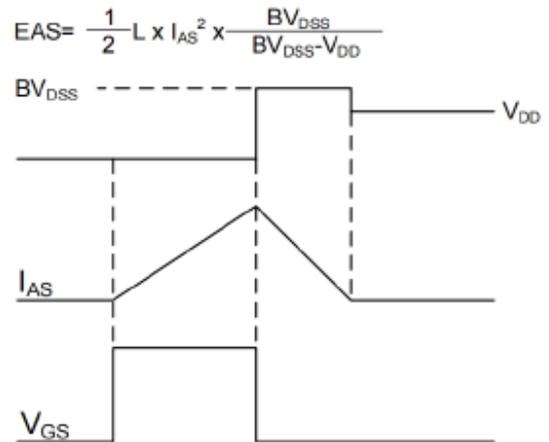
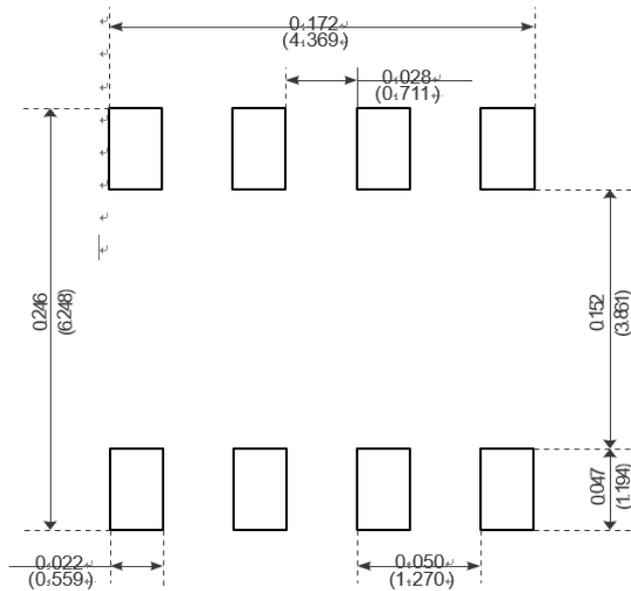
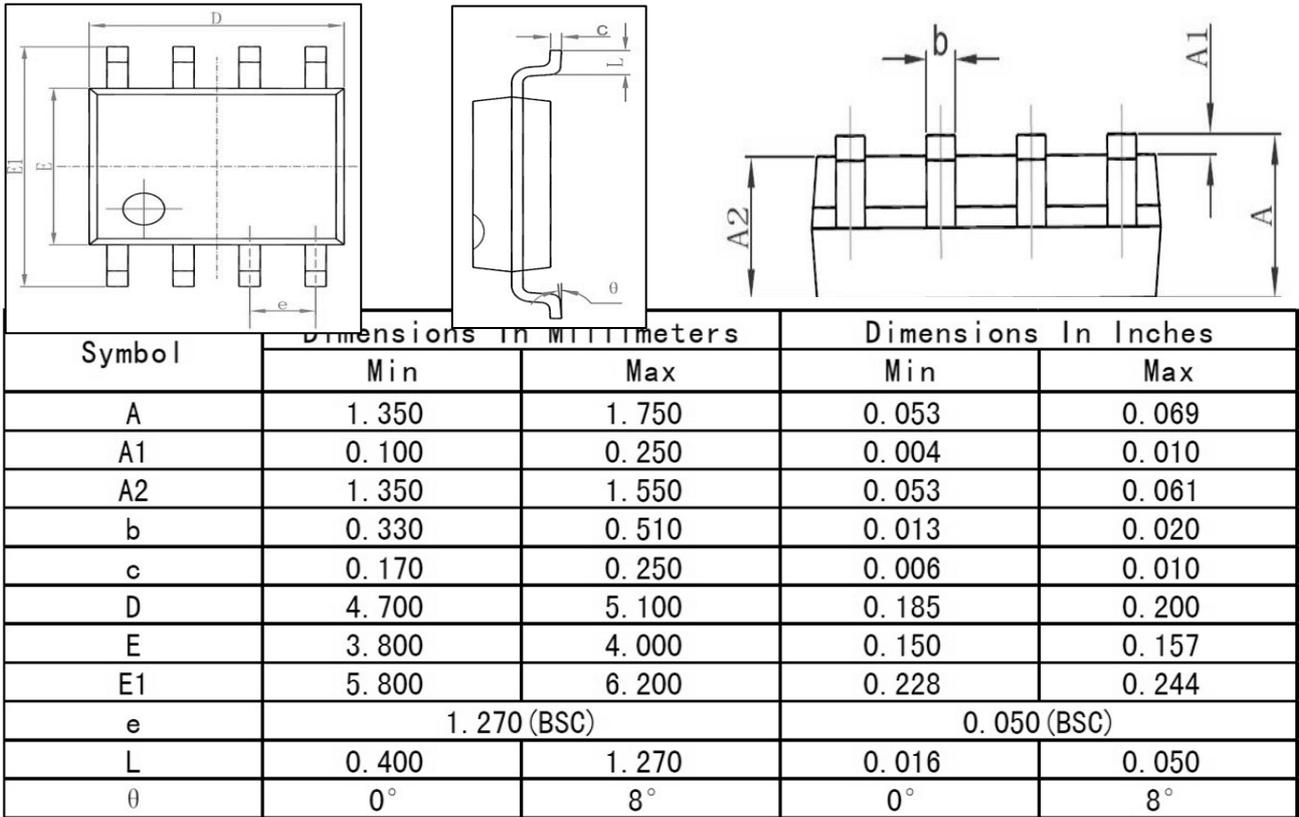


Fig.11 Unclamped Inductive Switching Waveform

Package Mechanical Data-SOP-8



Recommended Minimum Pads