

General Description

The MY30P02NE3 is the single P-Channel logic enhancement mode power field effect transistors to provide excellent $R_{DS(on)}$, low gate charge and low gate resistance.

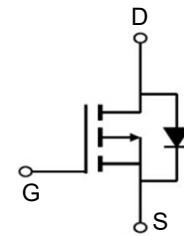
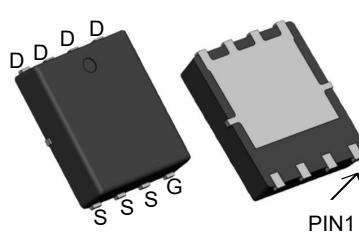


Features

$X_{F(U)}$	-20	X
I_F	-30	C
$T_{F(U)QP} + CVXI U? -4.5X+$	10	o á
$T_{F(U)QP} + CVXI U? -2.5X+$	13	o á

Application

- Battery protection System
- Switching power supply, SMPS
- DC/DC Converter
- DC/AC Converter
- Load Switch



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY30P02NE3	PDFN3*3-8L	MY30P02NE3	5000

Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V _{DS}	Drain- Source Voltage	-20	V
V _{GS}	Gate- Source Voltage	± 20	V
I _D @T _A =25°C	Drain Current ³ , V _{GS} @ 10V	-30	A
I _D @T _A =70°C	Drain Current ³ , V _{GS} @ 10V	-18	A
I _{DM}	Pulsed Drain Current ¹	-68	A
P _D @T _A =25°C	Total Power Dissipation	12	W
T _{TSG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C
R _{thj-c}	Maximum Thermal Resistance, Junction- case	18	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction- ambient ³	12	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain- Source Breakdown Voltage	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=-250\mu\text{A}$	-20	-	-	V
RDS(ON)	Static Drain-Source On-Resistance ²	$\text{V}_{\text{GS}}=-4.5\text{V}, \text{I}_D=-10\text{A}$	-	10	15	$\text{m}\Omega$
		$\text{V}_{\text{GS}}=-2.5\text{V}, \text{I}_D=-8\text{A}$	-	13	18	$\text{m}\Omega$
VGS(th)	Gate Threshold Voltage	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=-250\mu\text{A}$	-0.4	-0.7	-1.0	V
g_{fs}	Forward Transconductance	$\text{V}_{\text{DS}}=-5\text{V}, \text{I}_D=-10\text{A}$	-	43	-	S
IDSS	Drain- Source Leakage Current	$\text{V}_{\text{DS}}=-15\text{V}, \text{V}_{\text{GS}}=0\text{V}$	-	-	-1	μA
IGSS	Gate- Source Leakage	$\text{V}_{\text{GS}}=\pm 12\text{V}, \text{V}_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Q_g	Total Gate Charge	$\text{I}_D=-10\text{A}$	-	35	-	nC
Q_{gs}	Gate- Source Charge	$\text{V}_{\text{DS}}=-10\text{V}$ $\text{V}_{\text{GS}}=-4.5\text{V}$	-	5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge		-	10	-	nC
td(on)	Turn-on Delay Time	$\text{V}_{\text{DS}}=-10\text{V}$	-	12	-	ns
t_r	Rise Time	$\text{I}_D=-10\text{A}$ $\text{R}_G=3.3\Omega$	-	40	-	ns
td(off)	Turn-off Delay Time	$\text{V}_{\text{GS}}=-4.5\text{V}$	-	30	-	ns
t_f	Fall Time		-	10	-	ns
C_{iss}	Input Capacitance	$\text{V}_{\text{GS}}=0\text{V}$	-	2000	-	pF
C_{oss}	Output Capacitance	$\text{V}_{\text{DS}}=-15\text{V}$ $f=1.0\text{MHz}$	-	690	-	pF
C_{rss}	Reverse Transfer Capacitance	$\text{I}_S=-10\text{A}, \text{V}_{\text{GS}}=0\text{V},$ $d\text{I}/dt=100\text{A}/\mu\text{s}$	-	590	-	pF
trr	Reverse Recovery Time		-	27	-	ns
Q_{rr}	Reverse Recovery Charge		-	17.8	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test

Typical Characteristics

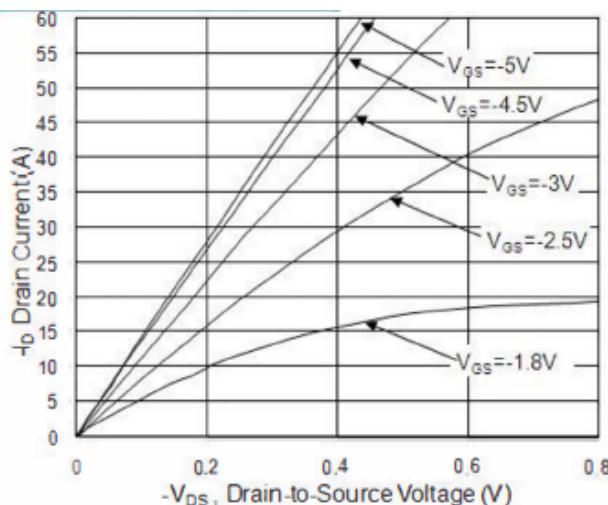


Fig.1 Typical Output Characteristics

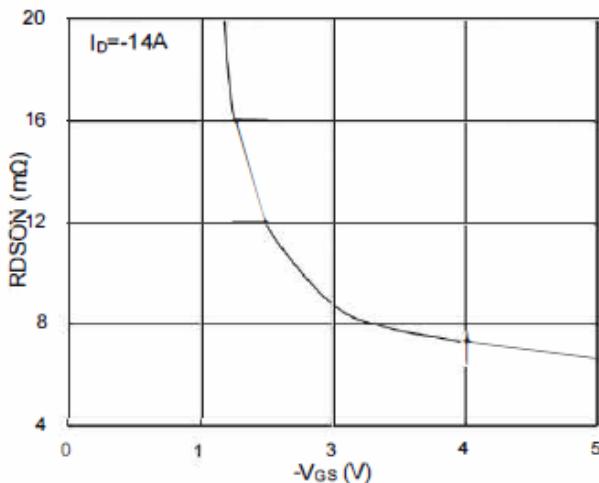


Fig.2 On-Resistance vs. G-S Voltage

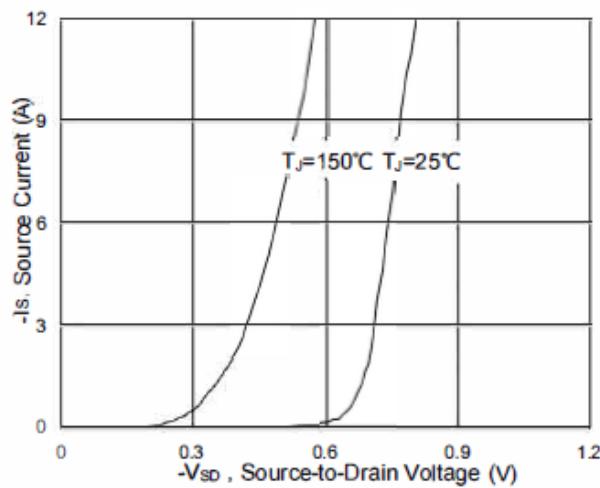


Fig.3 Forward Characteristics of Reverse

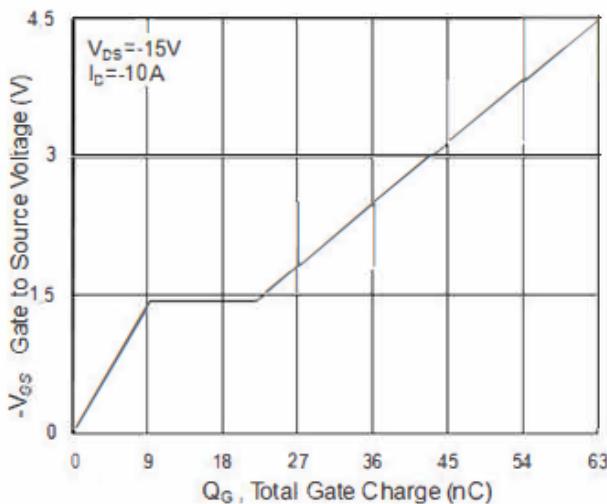
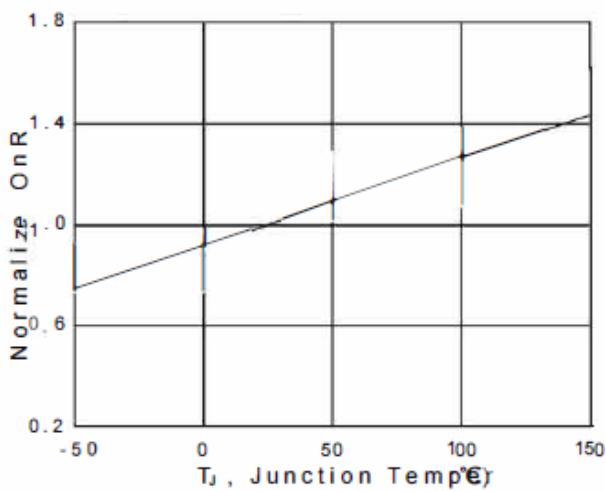
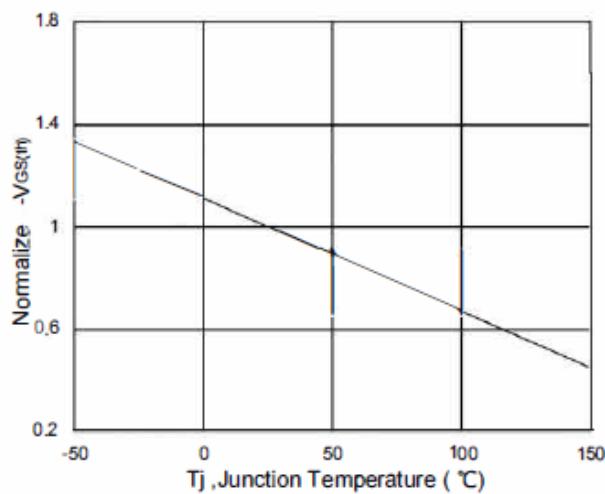


Fig.4 Gate-charge Characteristics



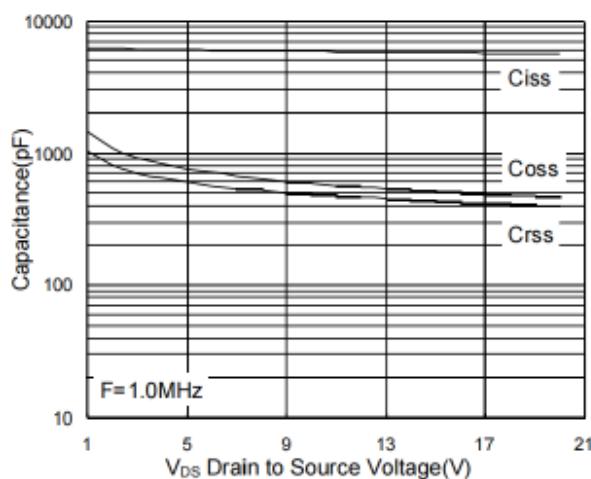


Fig.7 Capacitance

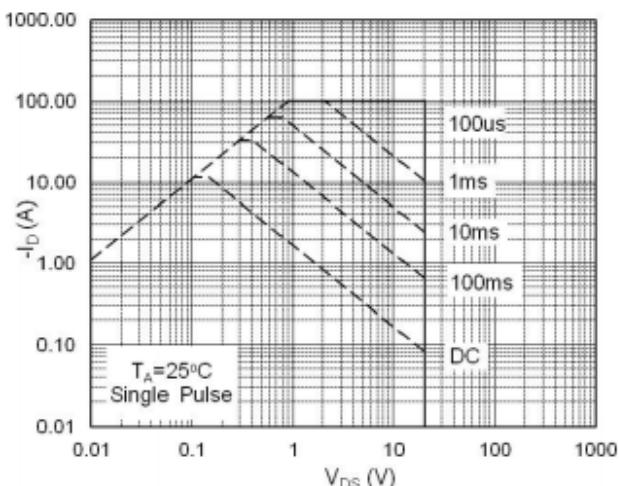


Fig.8 Safe Operating Area

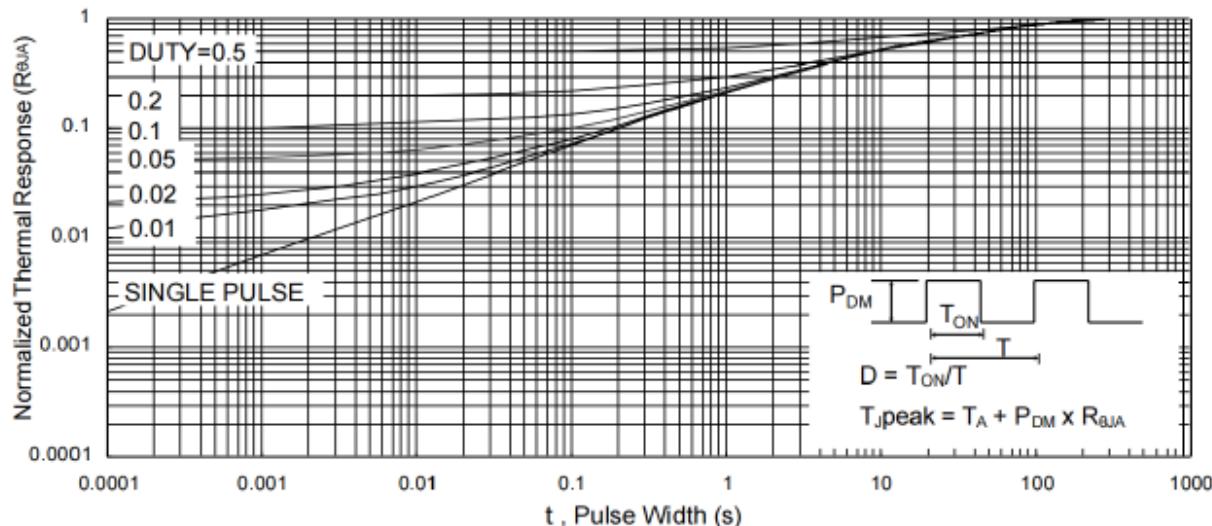


Fig.9 Normalized Maximum Transient Thermal Impedance

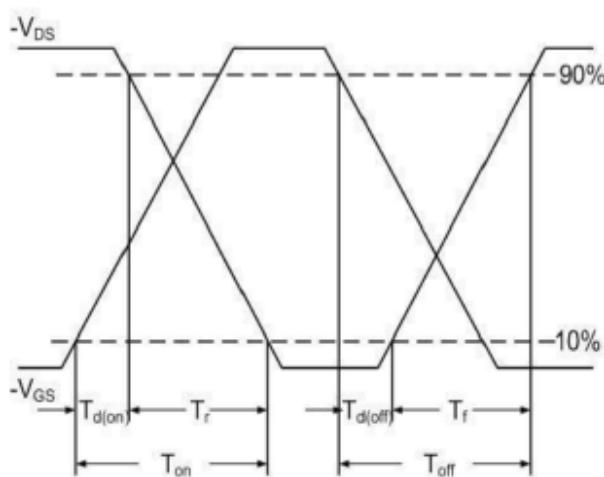


Fig.10 Switching Time Waveform

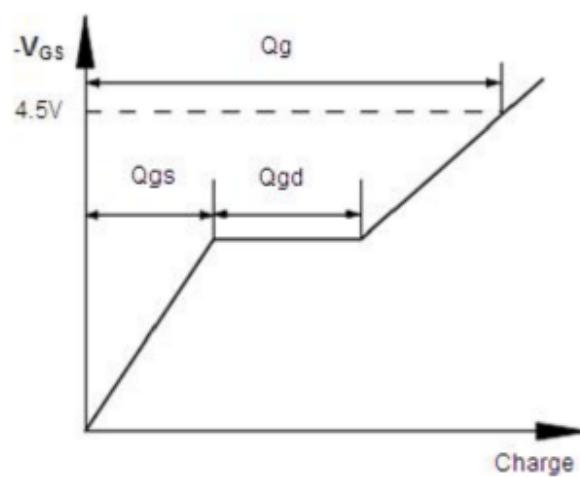
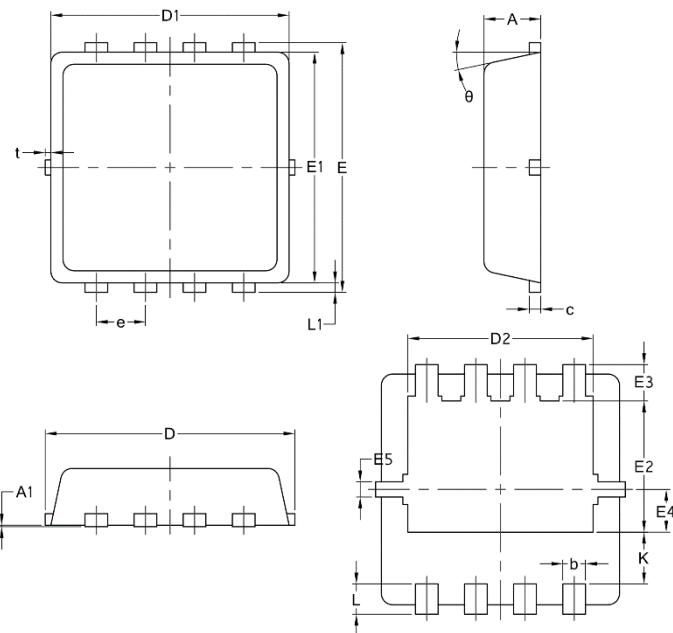


Fig.11 Gate Charge Waveform

Package Mechanical Data-DFN3*3-8L-JQ Single


Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14