

General Description

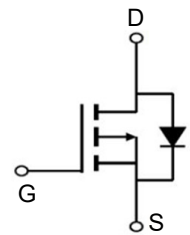
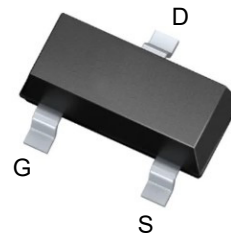
The MY3415 is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology.. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-line power loss are needed in a very small outline surface mount package.

Features

V_{DSS}	-20	V
I_D	-5	A
$R_{DS(ON)}(at V_{GS} = -4.5V)$	28	m Ω
$R_{DS(ON)}(at V_{GS} = -2.5V)$	36	m Ω

Application

- Power Management
- Portable Equipment
- DC/DC Converter



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY3415	SOT-23	3415	3000

Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter		Typical	Unit
V _{DSS}	Drain-Source Voltage		-20	V
V _{GSS}	Gate-Source Voltage		±8	V
I _D	Continuous Drain Current (T _C =25℃)	V _{GS} =-10V	-5	A
	Continuous Drain Current (T _C =70℃)		-3.5	A
I _{DM}	Pulsed Drain Current		-20	A
P _D	Power Dissipation	T _A =25℃	1.5	W
		T _A =70℃	0.9	
T _J	Operation Junction Temperature		150	℃
T _{STG}	Storage Temperature Range		-55~+150	℃
R _{θJA}	Thermal Resistance Junction to Ambient		120	℃/W

Electrical Characteristics ($T_J=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

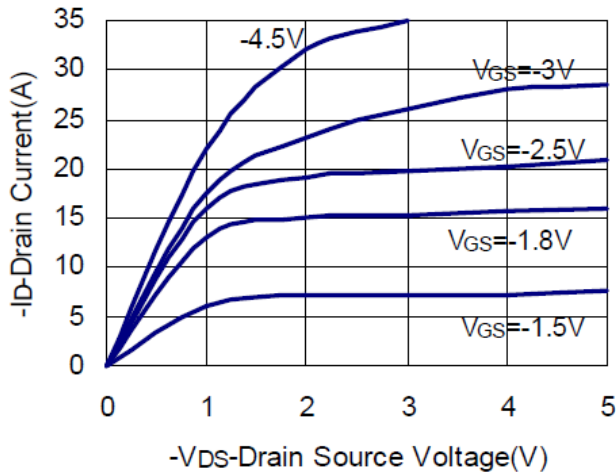
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.3		-1.0	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 8V$			± 10	μA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-12V, V_{GS}=0$			-1	μA
		$V_{DS}=-12V, V_{GS}=0$ $T_J=55^{\circ}\text{C}$			-5	
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=-4.5V, I_D=-4.3A$		28	38	$m\Omega$
		$V_{GS}=-2.5V, I_D=-3.0A$		36	45	
		$V_{GS}=-1.8V, I_D=-2.0A$		56	75	
		$V_{GS}=-1.5V, I_D=-1.0A$		85	110	
G_{fs}	Forward Transconductance	$V_{DS}=-5V, I_D=-4.0A$		22		S
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	$I_S=-1.0A, V_{GS}=0V$		-0.67	-1.2	V
Dynamic Parameters						
Q_g	Total Gate Charge	$V_{DS}=-10V$ $V_{GS}=-4.5V$ $I_D=-4.0A$		11.1		nC
Q_{gs}	Gate-Source Charge			3.1		
Q_{gd}	Gate-Drain Charge			2.4		
C_{iss}	Input Capacitance	$V_{DS}=-10V$ $V_{GS}=0V$ $f=1\text{MHz}$		989		pF
C_{oss}	Output Capacitance			167		
C_{rss}	Reverse Transfer Capacitance			75.5		
$T_{d(on)}$	Turn-On Time	$V_{DS}=-10V$ $I_D=-3.7A$		712		nS
T_r				1386		
$T_{d(off)}$	Turn-Off Time	$V_{GEN}=-4.5V$ $R_G=1\Omega$		9.1		
T_f				4		

Note: 1. Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

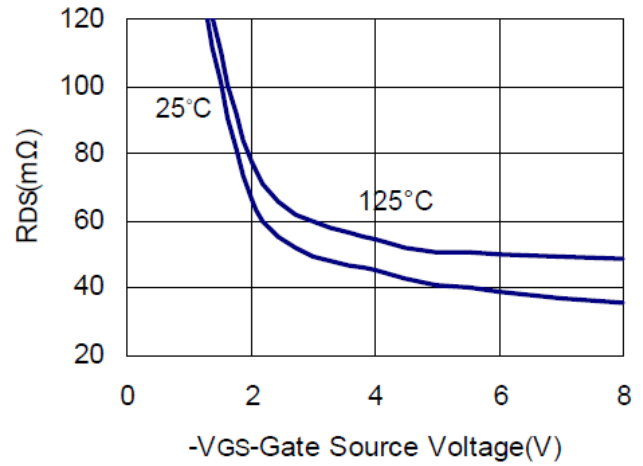
2. Static parameters are based on package level with recommended wire bonding

Switching Time Test Circuit and Waveforms

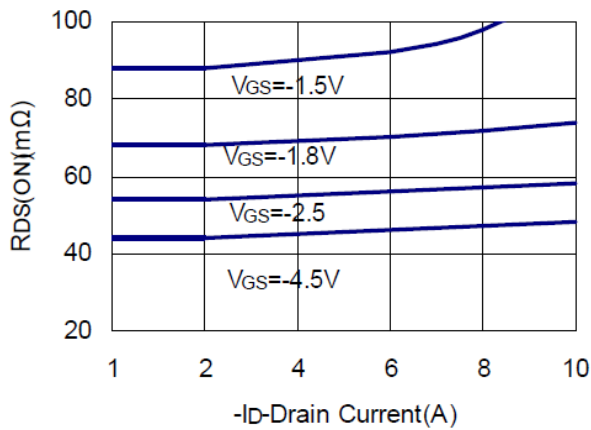
Output Characteristics



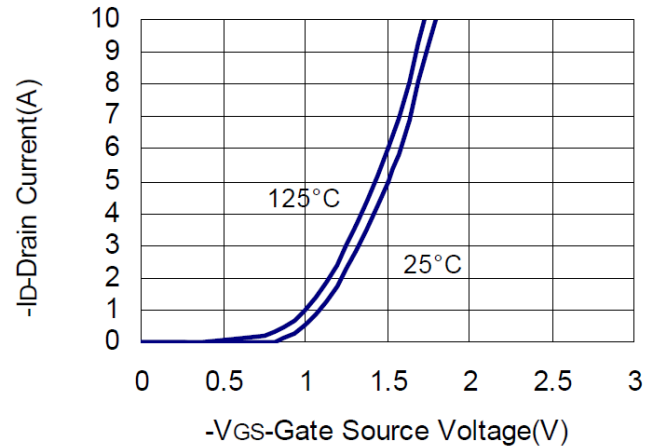
Drain-Source On Resistance



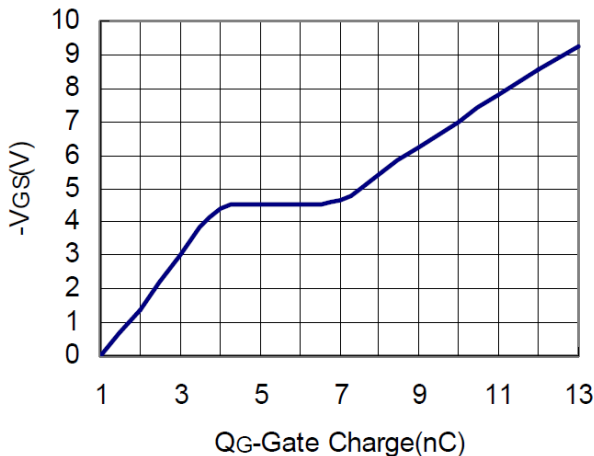
Drain Source On Resistance



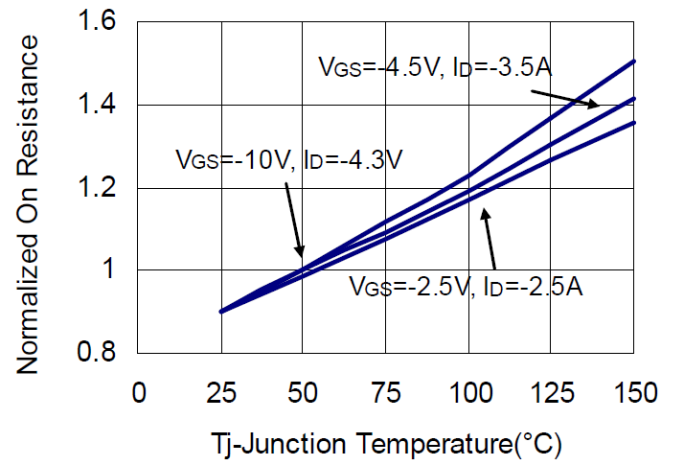
Transfer Characteristics

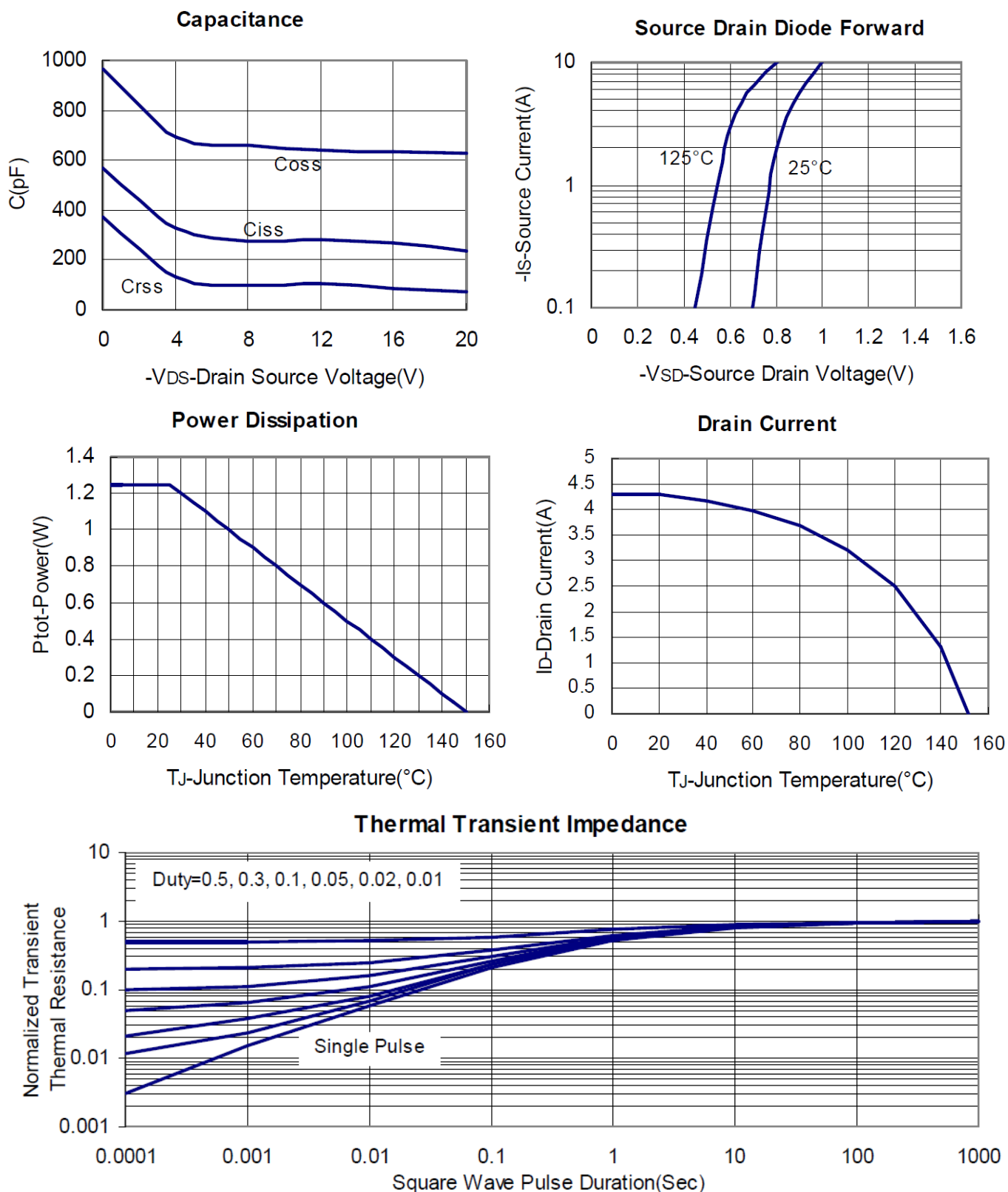


Gate Charge

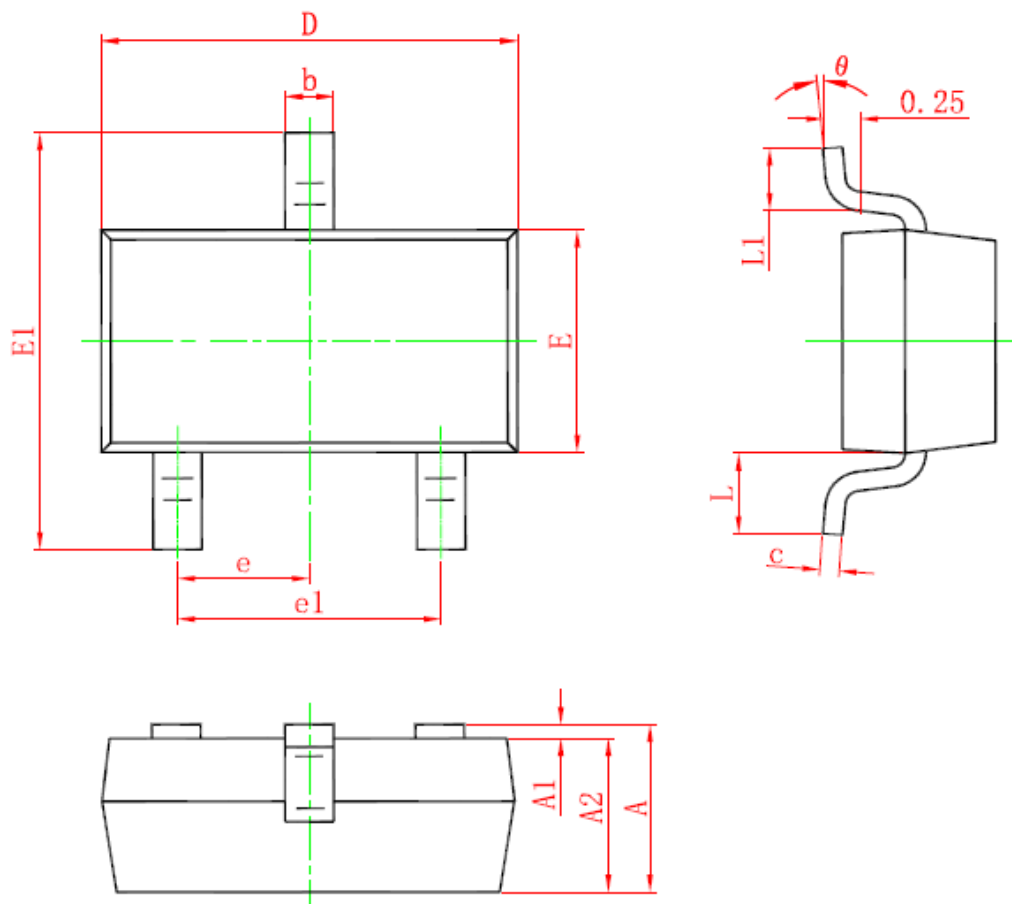


Drain Source Resistance





Package Mechanical Data-SOT-23



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°