

General Description

The MY70N10C use advanced SGT MOSFET technology to provide low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness and suitable to use in

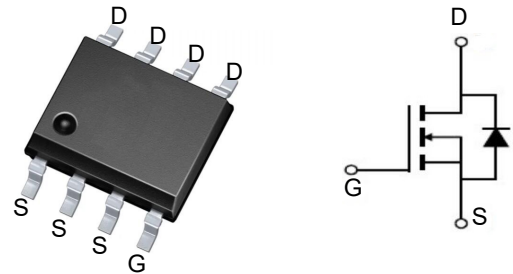


Features

V_{DSS}	100	V
I_D	80	A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	6.4	$m\Omega$
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	9.3	$m\Omega$

Application

- Battery protection
- Load switch
- Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY70N10C	SOP-8	MY70N10C	3000

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	100	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^\circ\text{C}$	I_D	68	A
Pulsed drain current ²⁾ , $T_C=25^\circ\text{C}$	I_D , pulse	180	A
Power dissipation ³⁾ , $T_C=25^\circ\text{C}$	P_D	125	W
Single pulsed avalanche energy ⁵⁾	EAS	100	mJ
Operation and storage temperature	T_{stg} , T_J	-55 to 150	$^\circ\text{C}$
Thermal resistance, junction-case	$R_{\theta JC}$	1	$^\circ\text{C/W}$
Thermal resistance, junction-ambient ⁴⁾	$R_{\theta JA}$	62	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$	100			V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$	1.2	2.0	2.5	V
Drain-source on-state resistance	$R_{DS(ON)}$	$V_{GS}=10\text{ V}$, $I_D=20\text{ A}$		6.4	7.7	m Ω
Drain-source on-state resistance	$R_{DS(ON)}$	$V_{GS}=4.5\text{ V}$, $I_D=15\text{ A}$		9.3	11.6	m Ω
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$			100	nA
					-100	
Drain-source leakage current	I_{DSS}	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$			1	μA
Input capacitance	C_{iss}	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$		2604		pF
Output capacitance	C_{oss}			361.2		pF
Reverse transfer capacitance	C_{rss}			6.5		pF
Turn-on delay time	$t_{d(on)}$	$V_{GS}=10\text{ V}$, $V_{DS}=50\text{ V}$, $R_G=2.2\text{ }\Omega$, $I_D=25\text{ A}$		20.6		ns
Rise time	t_r			5		ns
Turn-off delay time	$t_{d(off)}$			51.8		ns
Fall time	t_f			9		ns
Total gate charge	Q_g	$I_D=25\text{ A}$, $V_{DS}=50\text{ V}$, $V_{GS}=10\text{ V}$		49.9		nC
Gate-source charge	Q_{gs}			6.5		nC
Gate-drain charge	Q_{gd}			12.4		nC
Gate plateau voltage	$V_{plateau}$			3.4		V
Diode forward current	I_S	$V_{GS}<V_{th}$			60	
Pulsed source current	I_{SP}				180	A
Diode forward voltage	V_{SD}	$I_S=12\text{ A}$, $V_{GS}=0\text{ V}$			1.3	V
Reverse recovery time	t_{rr}	$I_S=12\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$		60.2		ns
Reverse recovery charge	Q_{rr}			106.1		nC
Peak reverse recovery current	I_{rm}			3		A

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25\text{ }^{\circ}\text{C}$.
- 5) $V_{DD}=50\text{ V}$, $R_G=25\text{ }\Omega$, $L=0.3\text{ mH}$, starting $T_J=25\text{ }^{\circ}\text{C}$.

Typical Characteristics

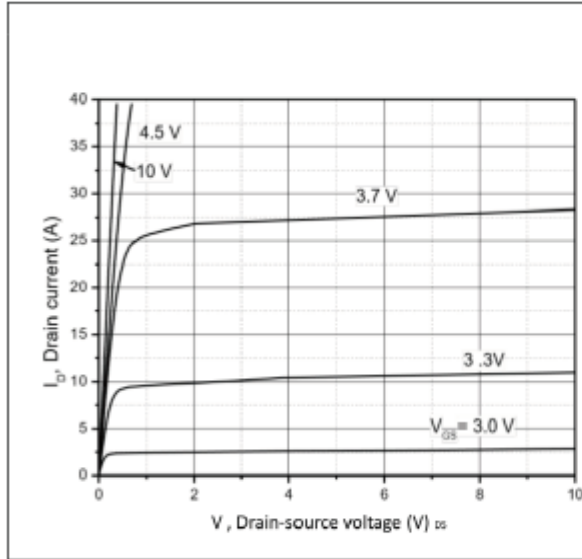


Figure 1, Typ. output characteristics

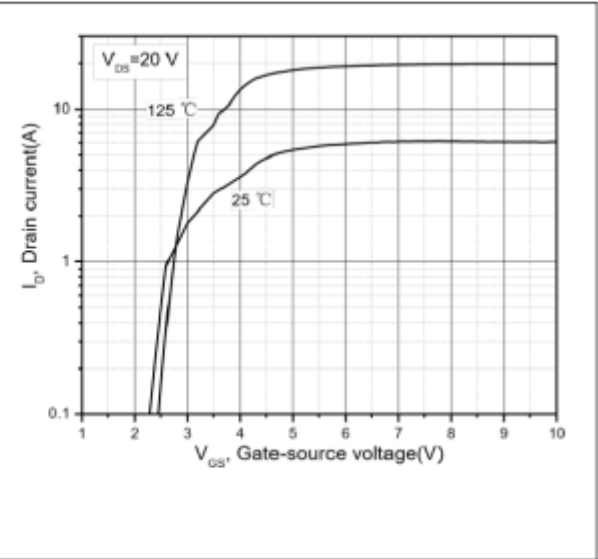


Figure 2, Typ. transfer characteristics

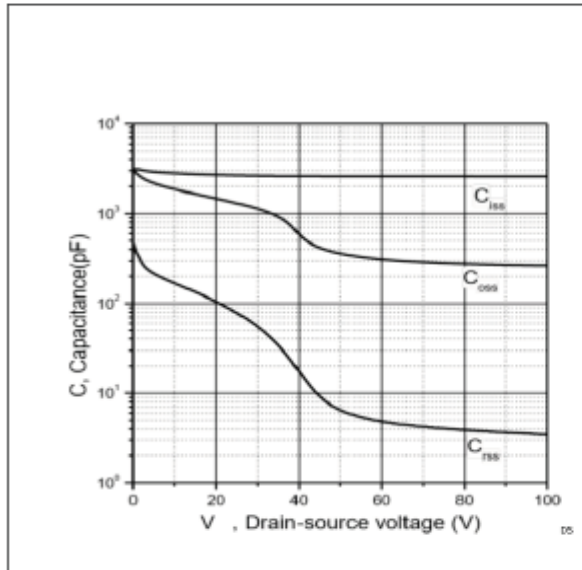


Figure 3, Typ. capacitances

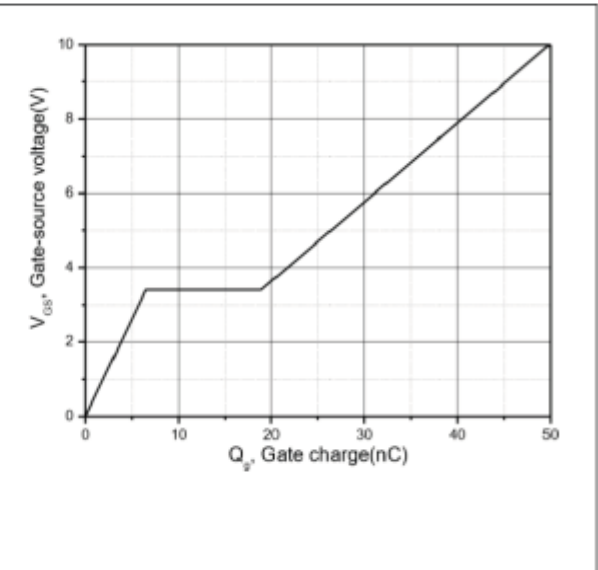


Figure 4, Typ. gate charge

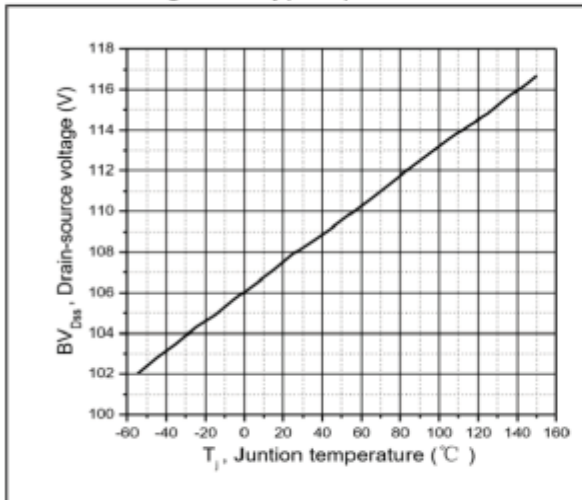


Figure 5, Drain-source breakdown voltage

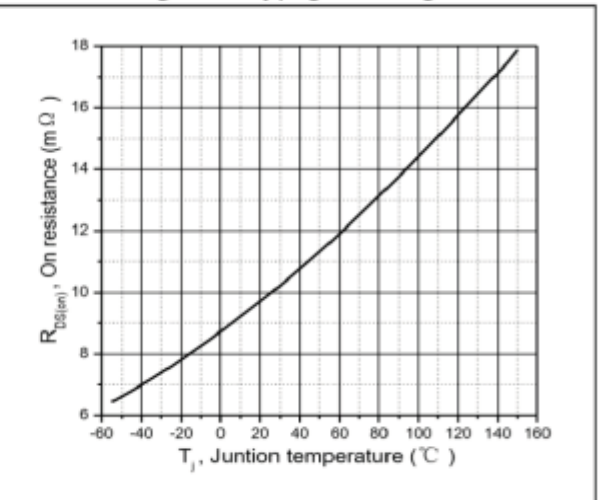


Figure 6, Drain-source on-state resistance

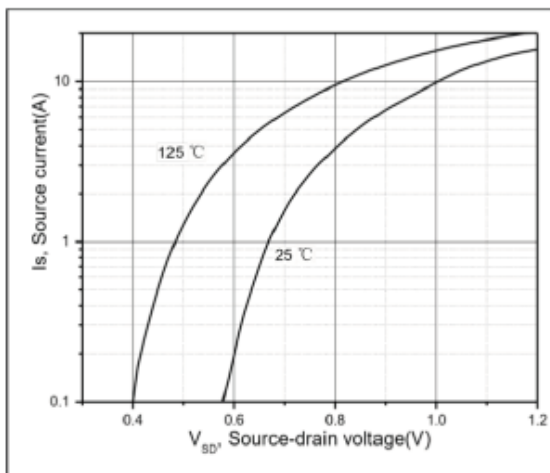


Figure 7, Forward characteristic of body diode

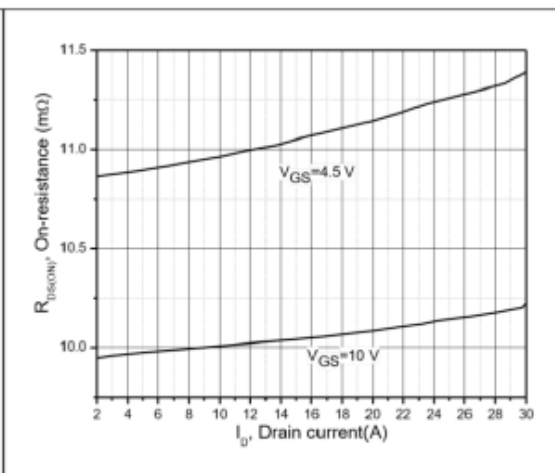


Figure 8, Drain-source on-state resistance

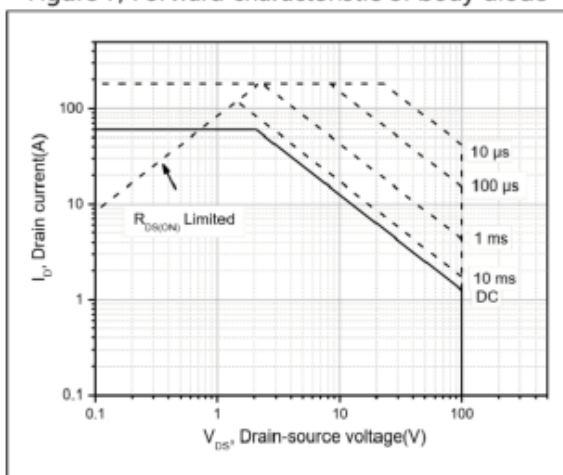


Figure 9, Safe operation area $T_C = 25\text{ }^{\circ}\text{C}$

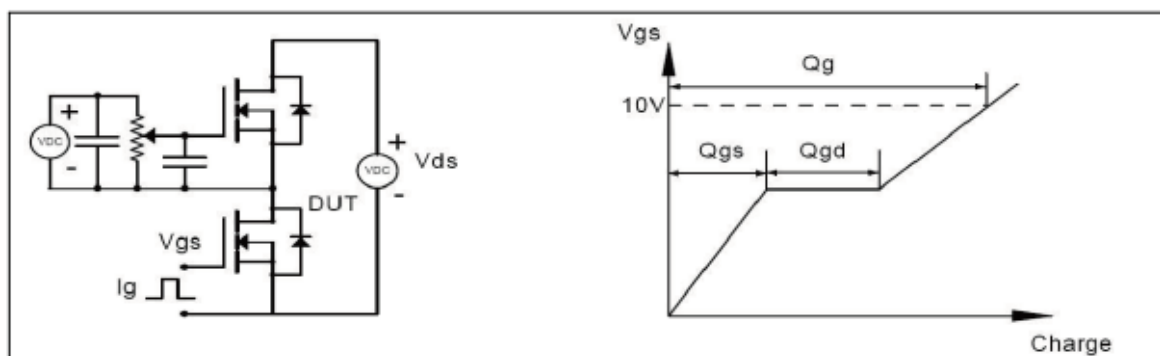


Figure 1. Gate charge test circuit & waveform

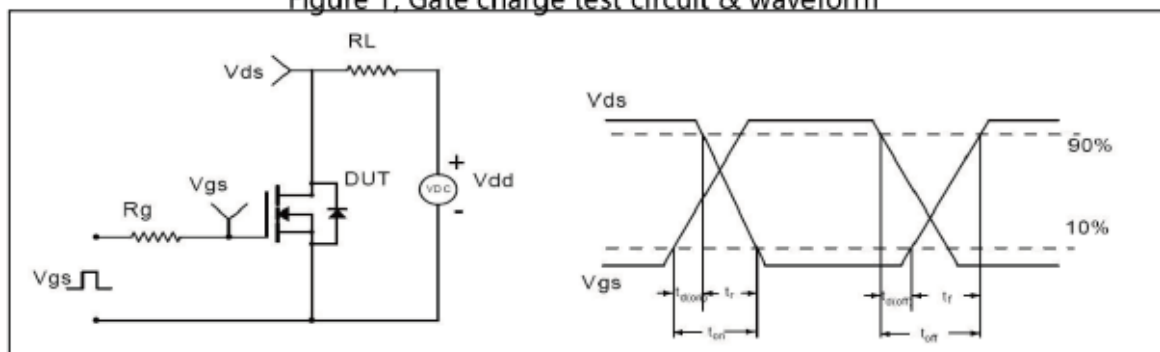


Figure 2. Switching time test circuit & waveforms

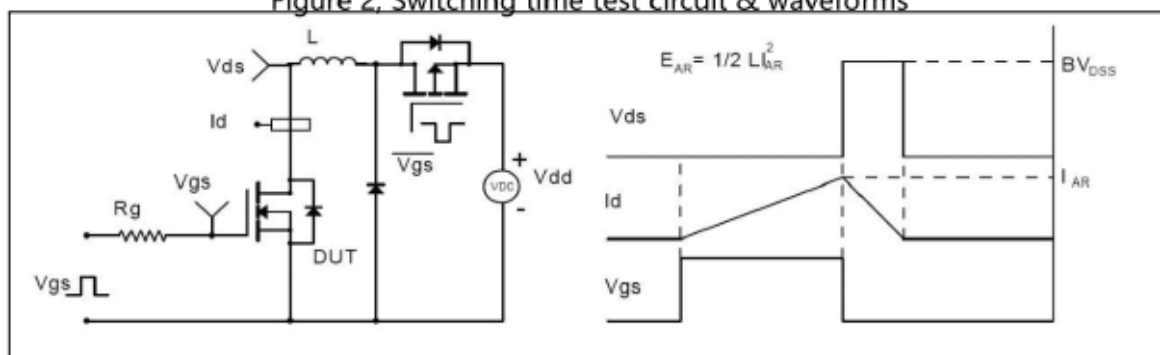


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

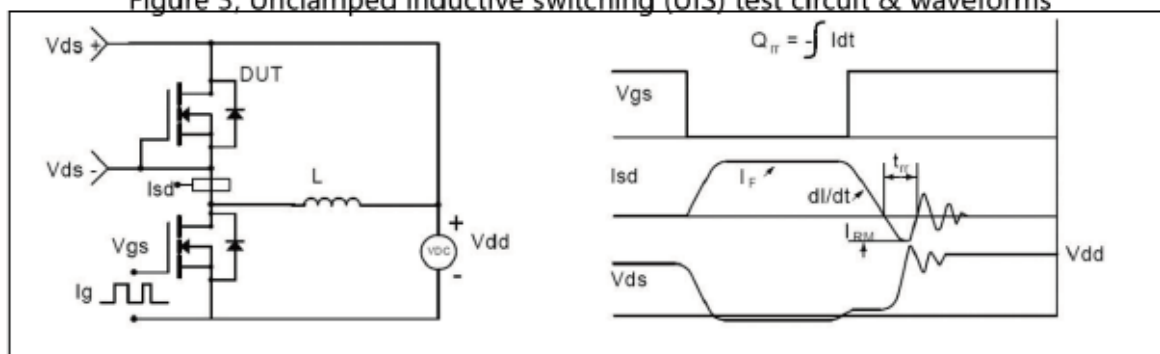
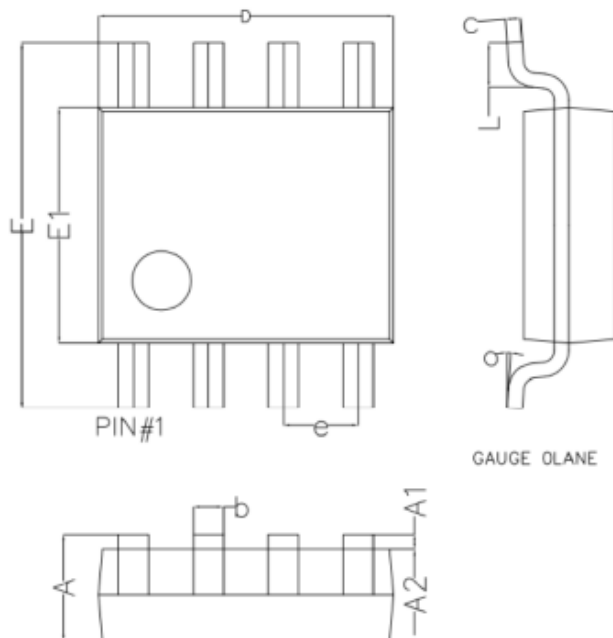


Figure 4. Diode reverse recovery test circuit & waveforms

Package Mechanical Data-SOP-8-JQ Single



Symbol	Dim in mm		
	Min	Nor	Max
A	1.350	1.550	1.750
A1	0.100	0.175	0.250
A2	1.350	1.450	1.550
b	0.330	0.420	0.510
c	0.170	0.210	0.250
D	4.800	4.900	5.000
e	1.270 (BSC)		
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.400	0.835	1.2700
o	0°	4°	8°